UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,071,069 B2
APPLICATION NO. : 10/743247
DATED : July 4, 2006
INVENTOR(S) : Chong Foong Tan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

* Claim 11, col. 9, line 36, step (d), "SDF ," changed to --SDE--.

* Please replace the entire Issued Claim 20, starting at col 10, lines 15 to 48 with the following:

--20. A method for a pocket implant comprising:
a) providing a gate structure on a semiconductor substrate comprised with a first conductivity type dopant;
b) performing a pocket amorphizing implantation procedure to implant ions of a first conductivity type to form a pocket implant region adjacent to said gate structure, an amorphous pocket region and pocket interstitials under the amorphous pocket region;
c) performing a shallow amorphizing implant to form an amorphous shallow implant region and shallow implant interstitials; the amorphous shallow implant region being formed at a second depth above said amorphous pocket region;
the substrate above the amorphous shallow implant region remains crystalline;
(1) said amorphous shallow implant region is formed at a minimum depth of about 8 nm and a maximum depth of 20 nm below the substrate surface; said amorphous shallow implant region has a thickness between 5 and 10 nm;

d) performing a SDE implant to form SDE regions of a second conductivity type, in an area of said semiconductor substrate not covered by said gate structure, with said SDE regions located in a top portion of said pocket region;
e) forming spacers on the sidewalls of the gate structure;
f) performing a S/D implant procedure to form Deep S/D regions;

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,071,069 B2
APPLICATION NO. : 10/743247
DATED : July 4, 2006
INVENTOR(S) : Chong Foong Tan et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

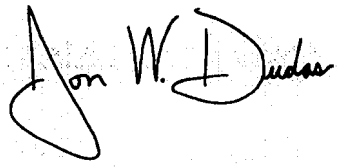
* Please replace the entire Issued Claim 20, starting at col 10, lines 15 to 48 with the following: (cont'd)

g) performing an anneal procedure comprised of a first soak step and a second spike step to recrystalilze the amorphous shallow implant region and said amorphous pocket region; whereby said shallow amorphous implant region reduces the defects from the pocket implantation;

(1) the anneal procedure comprises (1) a soak step at a temperature between 600 and 800 °C for a time between 10 and 30 seconds and (2) a spike step where the temperature ramps up to a peak temperature between 1000 and 1100 °C and a ramp down from said peak temperature to a temperature below 800 °C; said ramp up and ramp down have a rate between 200 and 300 degree° C per minute. --

Signed and Sealed this

Fifteenth Day of May, 2007



JON W. DUDAS
Director of the United States Patent and Trademark Office